S510

Semiconductor Reliability Test System

- Optimized for NBTI and TDDB testing of 65nm gate dielectric structures
- Speeds data collection for reliability modeling
- Boosts throughput by automating parallel on-wafer testing
- Highly scalable system provides 20 or more parallel stress/measure channels
- Provides an independent stress/measure channel for each test structure

APPLICATIONS

- Parallel Wafer Level Reliability testing
  - NBTI
  - TDDB
- Other Wafer Level Reliability testing
  - CHC (HCI)
  - Charge to breakdown
  - Electromigration

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Acquiring the masses of reliability data needed for modeling in a timely manner is more critical than ever because new materials and shrinking device dimensions demand that material and device engineers gain a better understanding of the behavior of gate dielectrics. Devices built using the new high κ materials are being pushed into production quickly, so there's less time available for reliability/lifetime assessment, process development, and process integration. In the past, stress-switch-measure testing was the standard approach to Negative Bias Temperature Instability (NBTI) and Time Dependent Dielectric Breakdown (TDDB) testing. However, this configuration is limited to measuring one or two devices at once, so it can't provide the amount of data required to keep pace with today's shorter development cycles. Keithley's S510 Automated WLR Tester takes a new approach to reliability testing. Dedicated source/measure channels allow the S510 to provide statistically significant quantities of data in as little as one-third the time required by a typical stress-switch-measure system. Unlike systems configured from expensive Source-Measure Units (SMUs) with wide measurement ranges, the S510's high speed channels offer targeted sourcing and measurement ranges, focused specifically on parallel NBTI and TDDB testing requirements.

New Reliability Models for New Technologies

The S510 makes it possible to acquire the measurement data necessary for lifetime characterization and reliability modeling of 65nm ULSI CMOS silicon devices far more quickly than earlier methods. In addition to solving a number of difficult measurement problems, the S510 incorporates high throughput system automation, including support for fully automatic wafer probers. The S510 includes high speed parallel SMUs to:

- Minimize device relaxation problems that plague NBTI testing.
- Allow every device to be monitored independently during stress intervals.
- Provide independent stress conditions for each test structure.
- Gather statistically significant quantities of data for device lifetime prediction and modeling.
- Maximize test throughput by characterizing up to 72 TDDB test structures or 36 NBTI test structures simultaneously.

In addition to the high speed parallel SMUs, the S510 design incorporates high resolution SMUs for expanded WLR testing capabilities. Combining the high resolution and high speed parallel SMUs provides an ideal "all-in-one" solution for pre- and post-characterization of the test structures, as well as seamless stress/measure cycling.

NBTI Testing

NBTI is a phenomenon where a change in a pMOS FET's gate-channel interface leads to degradation in pMOS device performance. This degradation is typically tracked as the increase of the transistor threshold voltage (V_T) and decrease of the drain current (I_D). Although there's no industry standard for NBTI testing, most organizations employ similar parameters and methods. The test for NBTI involves a stress/measure cycle, alternating between a stress interval with a voltage on the gate (V_G) and a measure interval, where a V_G–I_D sweep or single-point measurement of I_D, is performed. Before and after the stress/measure cycling, the device is characterized to establish its initial and final performance. These characterizations may be more comprehensive than the intermediate measure intervals. Throughout the test, the device is held at an elevated temperature to decrease test times, which can range from a few hours to a few weeks.

The primary challenges associated with NBTI testing are controlling device relaxation and increasing test throughput. Immediately after the stress is removed from a device, it begins to relax, making it difficult to measure the degradation of the stressed part accurately. This immediate relaxation problem, which is common to all conventional stress-switch-measure systems, complicates both determining device lifetimes for existing technologies and developing models for new technologies and combinations of materials. In addition to device-level degradation, NBTI has performance implications at the product or chip level.

Conventional stress-switch-measure methods use a single SMU to stress all DUTs in parallel. Characterization during the measure interval is done sequentially; each DUT is switched from the stress SMU to the measurement SMUs. **Figure 1** illustrates the drawbacks associated with the stress-

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Ordering Information

System Configurations

Call factory to discuss configuration options for the S510 Semiconductor Reliability Test System.

NBTI Test Challenges

NBTI Challenge	Conventional stress-switch-measure systems	S510
Device relaxation	Switching between stress SMUs and measure SMUs allows the device to relax.	Dedicated SMU-per-DUT-pin and system architecture provides seamless transition between source and measure, virtually eliminating relaxation.
Behavior during stress	No meaningful measurements possible during stress interval.	Each SMU has a dedicated A/D converter, so synchronized measurements are taken frequently during the stress interval.
Difficulty of acquiring statistically significant amounts of data	Must test for longer periods of time (i.e., 10× the data requires 10× the test time).	Parallel testing permits testing up to 36 DUTs simultaneously. Independent SMU-per-device architecture allows assigning unique test conditions for each DUT.

switch-measure method during a stress/measure cycle. **Figure 2** shows the stress/measure cycle performance of the S510 using dedicated SMUs, which provide seamless transitions between the stress interval and measure interval.

TDDB Testing

TDDB testing involves applying voltage stress over time at an elevated temperature in order to characterize the lifetime of the gate dielectric. Unlike NBTI, which is only concerned with device degradation, TDDB addresses both degradation and failure of the dielectric structure.

TDDB has similar pre- and post-stress measurement intervals to determine device characteristics. However, unlike the multiple stress/measure cycles of NBTI, TDDB consists of a single stress interval, which typically isn't interrupted by any measure intervals. During stress, only the gate current (I_G) is monitored.

The use of new materials and smaller device dimensions has led to a change in the dominant failure type from a hard breakdown to a soft breakdown. A hard breakdown is an abrupt and significant increase in I_G. A soft breakdown is seen as an increase in the noise of the signal (I_G), along with a gradual increase in I_G over time, possibly tens of seconds. Conventional stress-switch-measure systems can't provide meaningful I_G measurements of soft breakdowns on multiple devices, because multiple DUTs are sharing a SMU. Each DUT contributes to the total current measured and the breakdown of the first device obscures additional device breakdowns. Of course, if one of the gate currents begins to exhibit a precursor to failure, such as a slightly increased I_G or a change in the I_G signal noise, the shared measurement can't provide measurements accurate enough to detect it.

TDDB Test Challenges

TDDB Challenge	Conventional Stress-switch-measure systems	S510
Identifying soft breakdown	Sharing source/measure capability across multiple DUTs obscures soft breakdown and progressive breakdown events.	Dedicated A/D converter for each device provides immediate measurements; no need to wait for a multiplexed measurement.
Characterizing behavior during stress	No meaningful measurements possible during stress.	Each SMU has a dedicated A/D converter, so frequent measurements are taken.
Pinpointing device failures	Sharing source capability across multiple DUTs means that a DUT failure affects all DUTs connected in parallel.	SMU-per-device-pin design means a failure on one device does not affect other DUTs.
Acquiring statistically significant quantities of data	Must test for longer periods of time (i.e., 10× the data requires 10× the test time).	Parallel SMUs permit testing up to 72 DUTs simultaneously. Independent SMU permits assigning unique test conditions for each DUT.

SMU-Per-Device Architecture

The S510 takes advantage of the Model 4500's high channel count, parallel SMU-per-device-pin architecture. Conventional systems typically use switching to multiplex or "share" a single SMU's sourcing-and-measurement capability among all the devices being tested. However, this configuration has significant drawbacks when testing leading-edge and developmental structures with dimensions of less than 90nm or those fabricated from new materials. A variety of test challenges are associated with

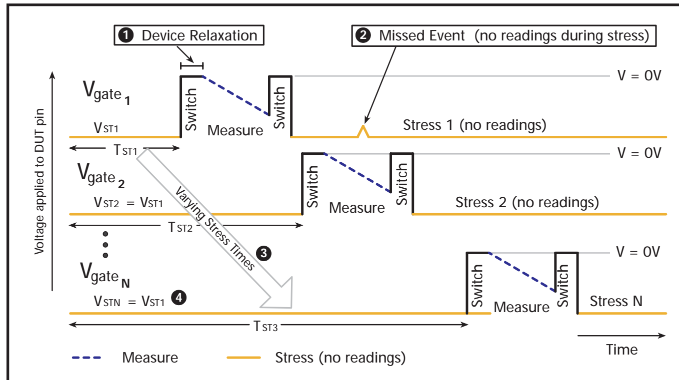


Figure 1. Example stress/measure cycle for a stress-switch-measure approach. Note: (1) device relaxation, (2) missed event during stress on DUT #1, (3) different stress times for each DUT, (4) single V_{stress} voltage shared for all DUTs (i.e., $V_{ST1} = V_{ST2} = \ldots V_{STN}$). This is a simplified diagram showing the stress and measure on one pin per DUT; typical stress/measure configurations will have non-zero voltages on two or three of the four pins on a typical FET DUT.

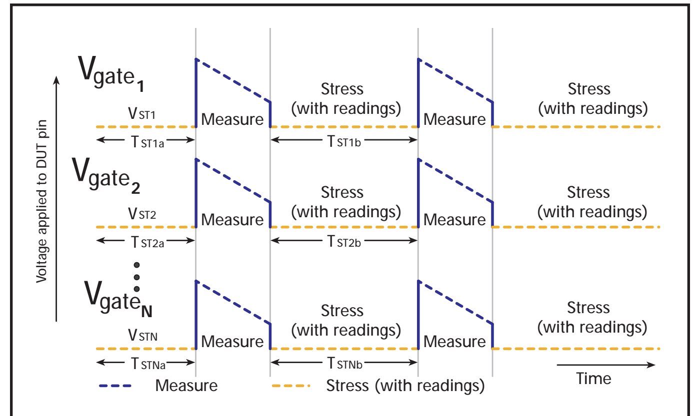


Figure 2. Example stress/measure cycle for dedicated SMU approach. Compare to Figure 1. Note that the time for each stress interval is the same and, that each voltage stress (V_{ST}) can have a unique value, R, and that readings are taken during the stress intervals.

sharing source and measure capabilities across all DUTs in an NBTI or TDDB test. The S510's dedicated source and measure capability, provided by the high speed parallel SMUs, eliminates the challenges associated with gate reliability testing on ULSI CMOS structures.

The high resolution SMUs are needed for characterization before and after stress/measure testing. These high resolution SMUs are also key for other reliability tests, such as HCI (CHC), Q_{BD} (charge to breakdown), and electromigration, in which continuous monitoring of device degradation is much less important. The high resolution SMU is ideal for these applications because the S510's expandable architecture makes it easy to add SMUs to characterize transistors and gate dielectric structures individually; it also offers the exceptional low current measurement sensitivity and fast autoranging applications of this type demand.

The S510 allows connecting either the high resolution SMUs or the high speed parallel SMUs to any DUT pin. A switch matrix provides sequential access to the high resolution SMUs for each DUT. A separate bypass switch connects each dedicated high speed parallel SMU to its pin. This flexibility allows switching in the most appropriate sourcing and measurement configuration for the application easily, choosing either high resolution characterization for HCI, Q_{BD}, and EM tests or the dedicated SMU capability required for gate dielectric reliability testing (Figure 3).

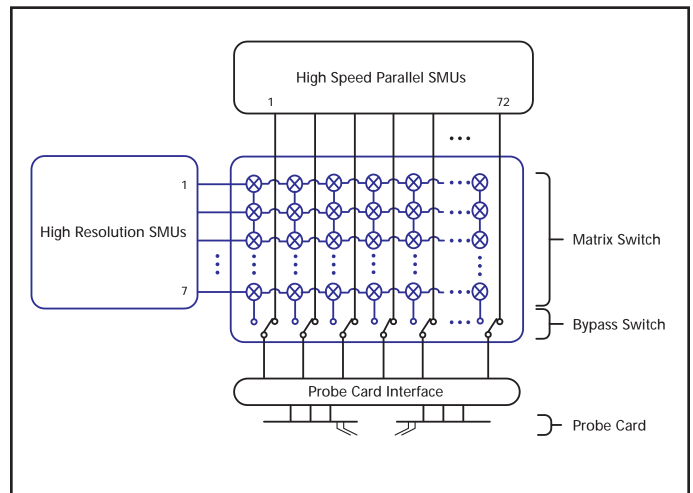


Figure 3. A bypass switch isolates the S510's high resolution channels while the high speed parallel channels are performing NBTI and TDDB testing. When the high resolution channels are in use, the bypass switch isolates the high speed parallel channels. This prevents interference between the two SMU types during system operation. The user supplies the probe card and interface.

S510 Software

The S510 incorporates several different software components to address a variety of system functions:

- **Keithley Test Environment (KTE) for fully automatic operation**

  The same powerful production-grade test executive that drives Keithley's automated parametric test systems powers the S510, too. KTE is the culmination of nearly four decades of experience in automated parametric tester design and is used in semiconductor fabs around the world. This test environment makes "lights-out" automation possible in the technology development lab, as well as on the fab floor, and supports complex sampling plans at the cassette, wafer, and site level.

- **Keithley Test Environment Interactive (KTEI V5.0) for interactive graphical user interface**

  KTEI, the test executive for the Model 4200, has become the industry's most popular interactive GUI software for semiconductor parametric analysis. It's widely used in applications like device characterization, materials research, device reliability, and failure analysis. A variety of Interactive Test Modules (ITMs) allow simple point-and-click test sequence development and operation.

- **S510 Parallel WLR Module**

  The S510's dedicated parallel WLR module is optimized for NBTI and TDDB testing on up to 72 high speed parallel channels. This flexible configuration can accommodate many stress/measure tests. Each device pin can be assigned unique stress and measure values; global variables can be used to assign the same conditions to a group of devices.

Continuum of WLR Solutions

Keithley scalable WLR offerings provide a cost-effective migration path from existing technology nodes to materials and devices under development.

4200-SCS: Contains the high resolution SMU capability for the S510, offering wide dynamic range SMUs that address the broadest range of technology nodes.

4500-MTS: Provides the S510's high speed parallel SMU capability, for addressing 90nm NBTI and TDDB WLR challenges.

S510: Packages the capabilities of the Model 4200 and the Model 4500 with the test horsepower of fully automatic wafer probers for 65nm gate dielectric WLR testing (**Figure 4**).

These solutions offer a cost-effective migration path by allowing significant equipment reuse as new reliability test needs evolve.

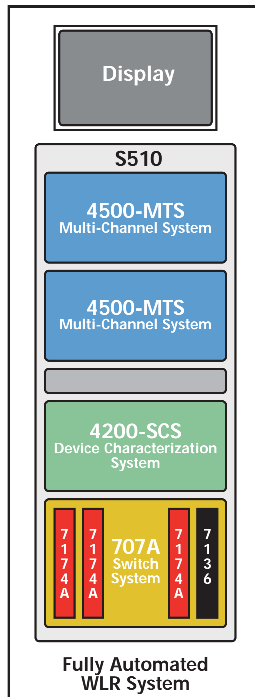


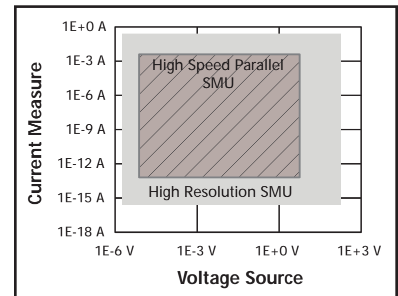
Figure 4. Keithley's S510 combines the high resolution SMUs of the Model 4200 and high speed parallel SMUs of the Model 4500.

S510 Condensed Specifications

The S510 has two types of SMUs, which provide different source and measure capabilities. The high resolution SMU has better low current measurement capability, while the high speed parallel SMU provides quick, independent and synchronous measurements on many channels. Both types of SMUs have independent source control and a dedicated A-to-D converter.

High resolution SMU	• 1fA measurement resolution • 100mA and 200V maximum output • Up to seven SMUs
High speed parallel SMU	• 100pA resolution • 10mA and 10V maximum output • Up to 72 channels, each with independent source and measure
Parallel testing	• Maximum of 72 channels provides - 36 DUTs for NBTI (2 High Speed Channels per DUT) - 72 DUTs for TDDB (1 High Speed Channel per DUT)
Switching matrix	• Permits either high resolution or high speed parallel connection to each pin • All paths active guarded • Up to 72 channels
Wafer interface	• One standard triax cable per pin • Supports multi-pin and multi-site probe cards
Prober support	All major semiconductor wafer probers are supported, including Accretech (TSK) UF3000, EG4080/4090/5 | 300, EG2001/4085, TSK APM-90A, TEL P-8/P-12XL. To determine if a particular prober is supported, contact your local sales representative.

All specifications apply at the end of the S510 triax cables.



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